

What is claimed is:

1. A scan test system for a semiconductor device,
comprising:

- 5 a first semiconductor device including a first analog
input/output pin existing on the analog input side thereof, a
first internal circuit, and a scan register connected between
said first input/output pin and said first internal circuit;
 a second semiconductor device including a second analog
10 input/output pin on the analog input side thereof, a second
internal circuit, and a scan register connected between said
second input/output pin and said second internal circuit; and
 an analog wiring connecting said first analog input/output
pin and said second analog input/output pin.

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2. The scan test system for a semiconductor device
according to Claim 1, wherein at least one of the first and second
semiconductor devices constitutes a register chain that
serially connects a plurality of the scan registers within the
20 device.

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3. The scan test system for a semiconductor device
according to Claim 2, wherein the scan register constituting
the register chain complies with the JTAG specification, and
25 constitutes a JTAG scan register, and the test system comprises
control means for controlling this JTAG scan register.

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4. A scan test system for a semiconductor device,
comprising:

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said semiconductor device including:

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